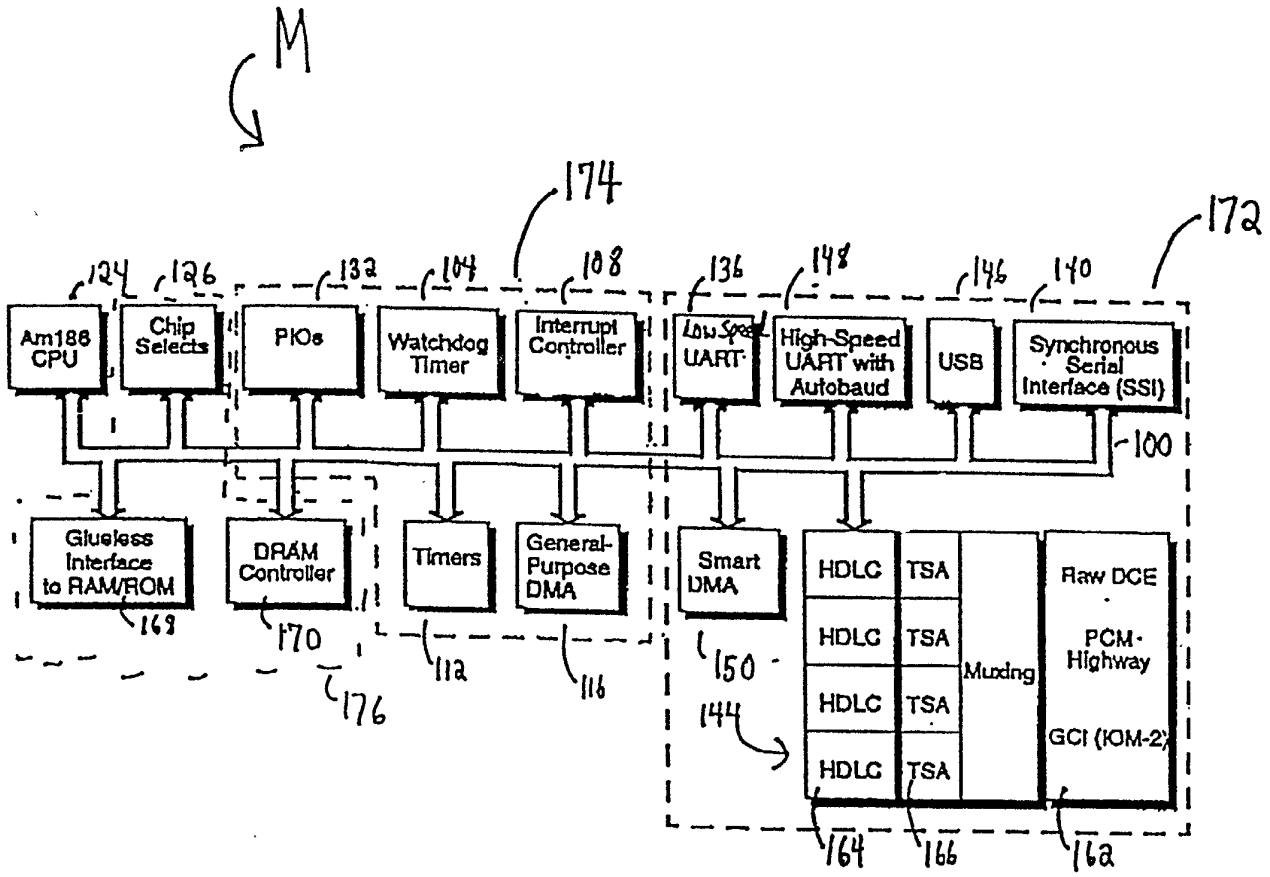
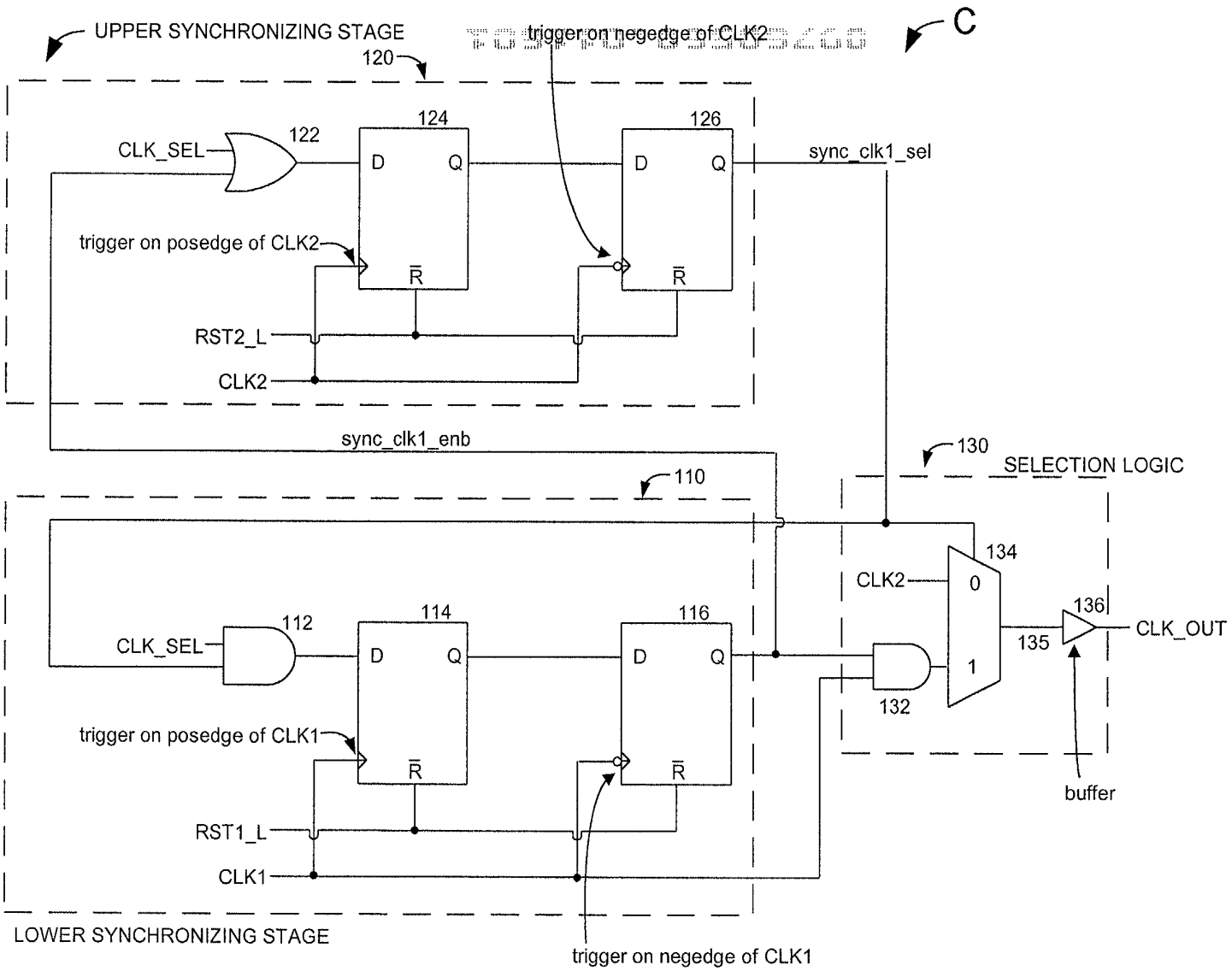

M
174
172
124
126
132
104
108
136
148
146
140
Am186 CPU
Chip Selects
PIOs
Watchdog Timer
Interrupt Controller
Low Speed UART
High-Speed UART with Autobaud
USB
Synchronous Serial Interface (SSI)
100
Glueless Interface to RAM/ROM
DRAM Controller
Timers
General-Purpose DMA
Smart DMA
HDLC
HDLC
HDLC
HDLC
TSA
TSA
TSA
TSA
Muxing
Raw DCE
PCM-Highway
GCI (IOM-2)
168
170
176
112
116
150
144
164
166
162

FIG. 1



Notes:

* RST2_L is system reset synchronized to CLK2.
* RST1_L is system reset synchronized to CLK1.
* CLK_SEL is an asynchronous signal.

Figure 2a

Synthesized (gate implementation) schematic from Verilog RTL

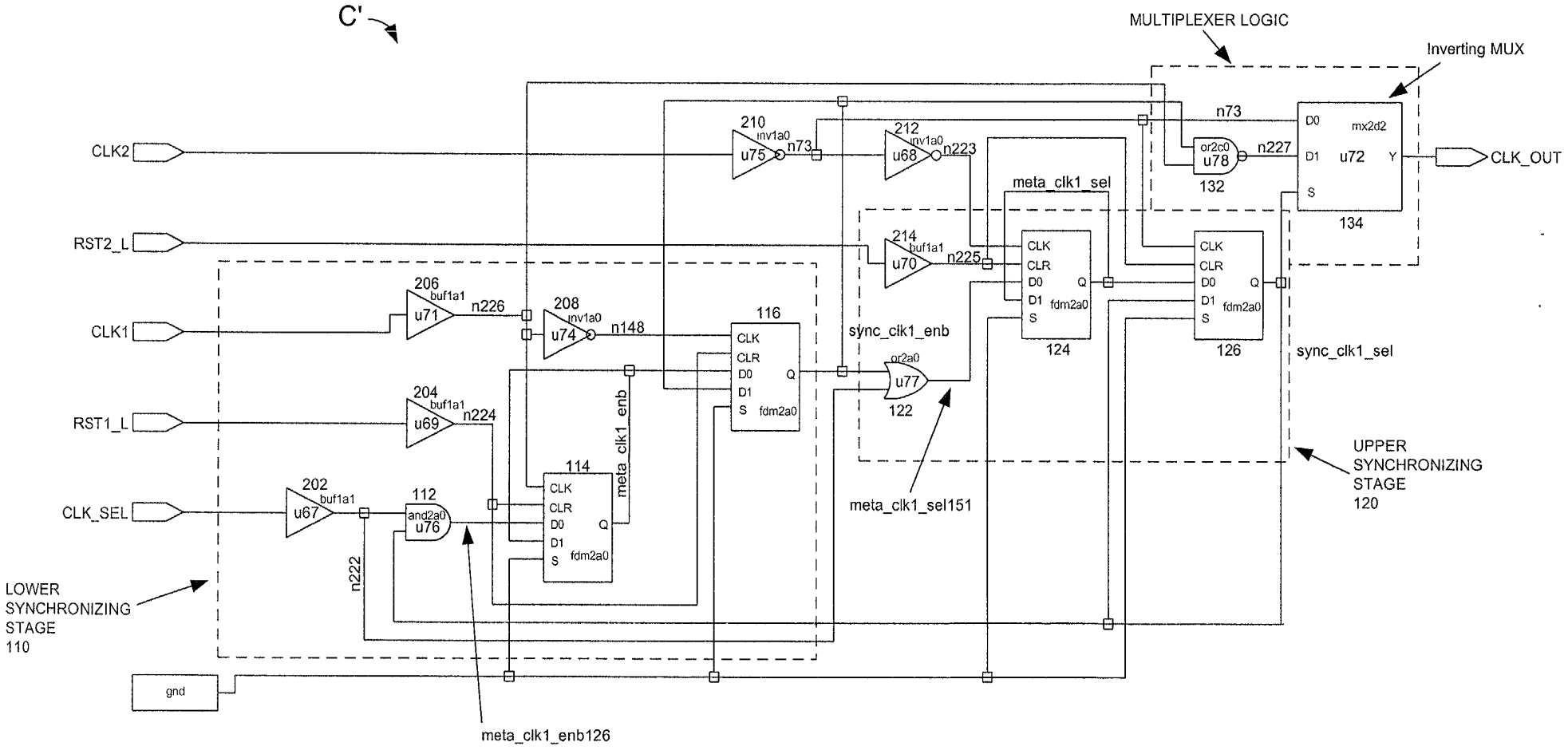
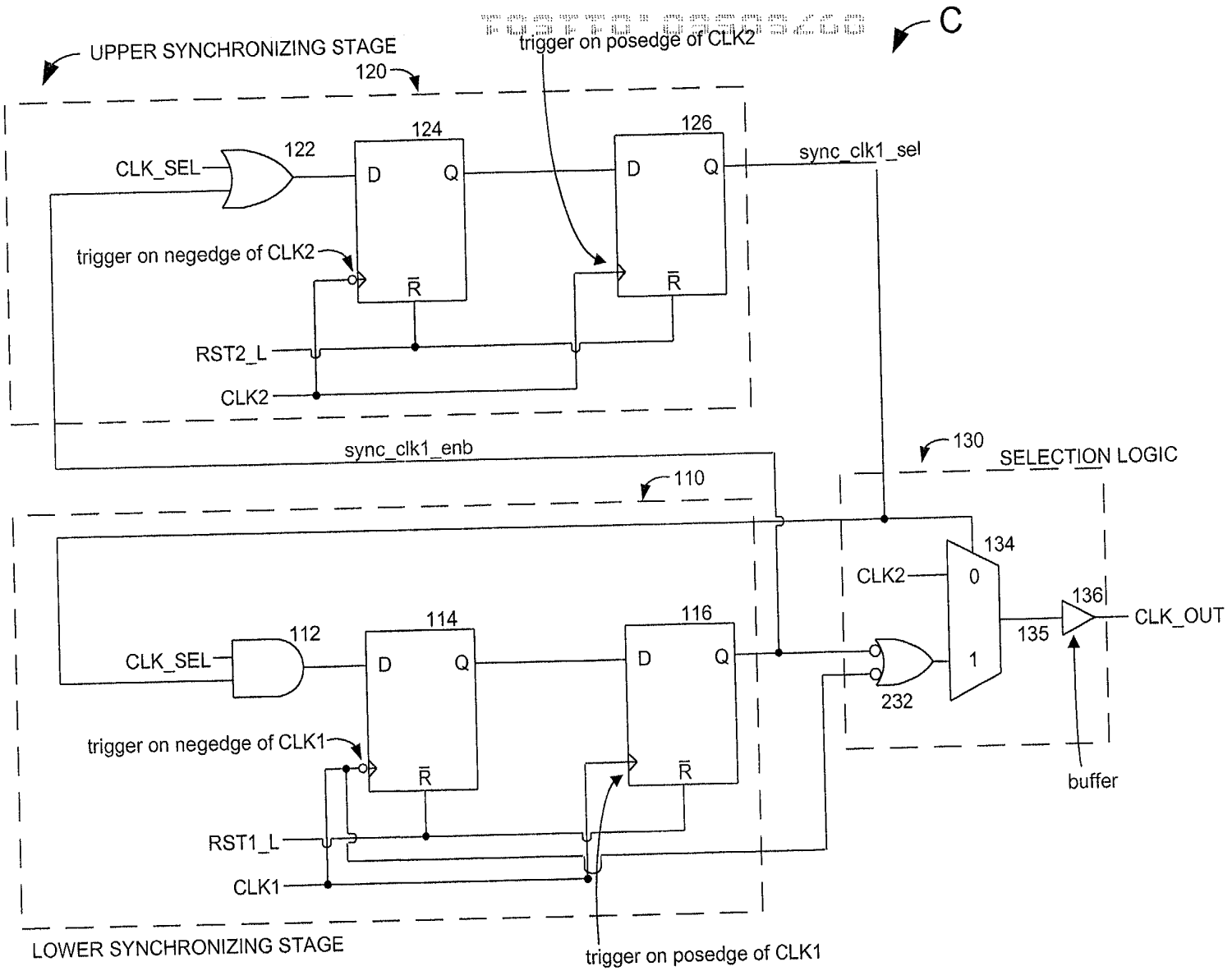


Figure 2b



Notes:

* RST2_L is system reset synchronized to CLK2.
* RST1_L is system reset synchronized to CLK1.
* CLK_SEL is an asynchronous signal.

Figure 2c

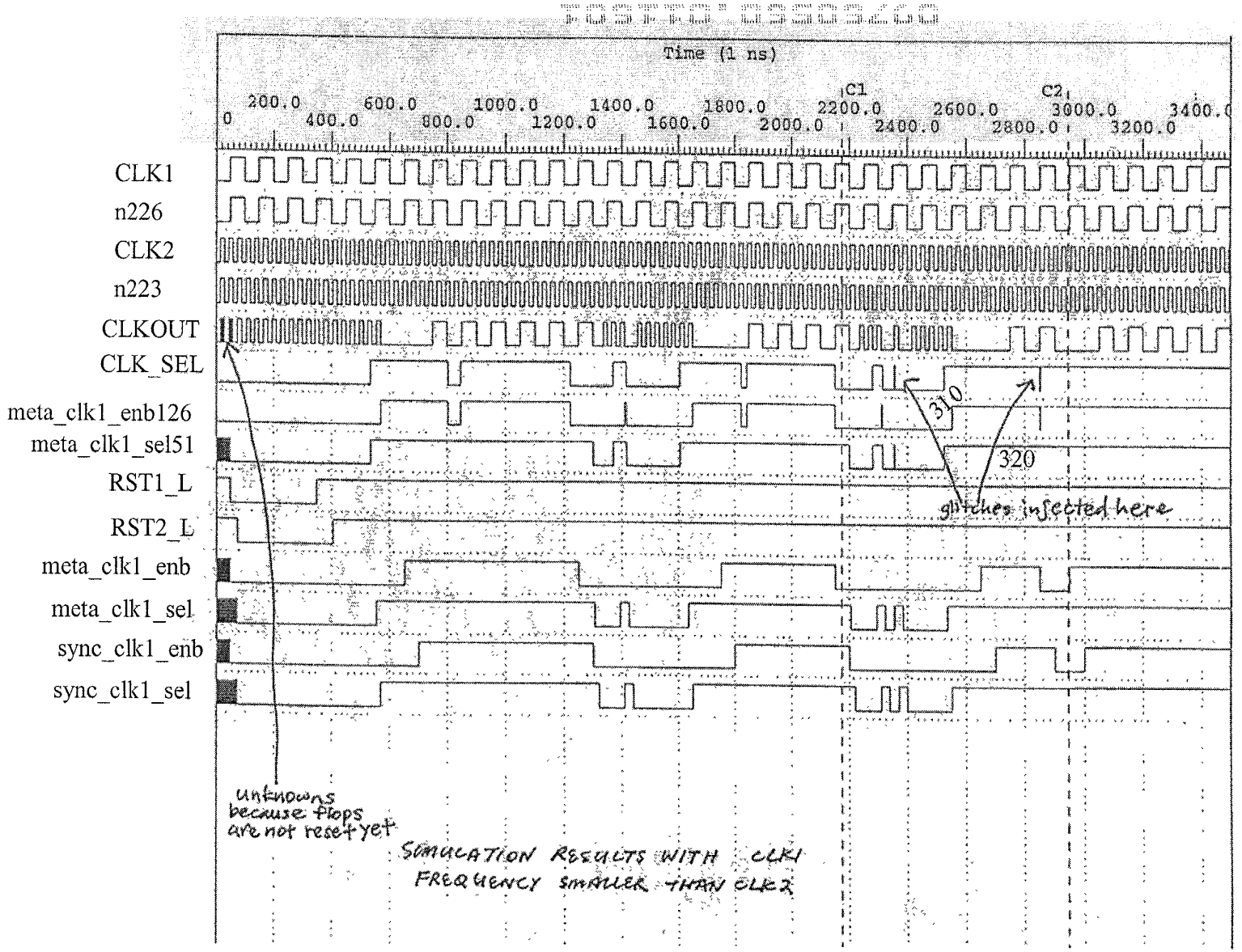

Time (1 ns)
C1
C2
0
200.0
400.0
600.0
800.0
1000.0
1200.0
1400.0
1600.0
1800.0
2000.0
2200.0
2400.0
2600.0
2800.0
3000.0
3200.0
3400.0
CLK1
n226
CLK2
n223
CLKOUT
CLK_SEL
meta_clk1_enb126
meta_clk1_sel51
RST1_L
RST2_L
meta_clk1_enb
meta_clk1_sel
sync_clk1_enb
sync_clk1_sel
310
320
glitches injected here
unknowns because flops are not reset yet
SIMULATION RESULTS WITH CLK1 FREQUENCY SMALLER THAN CLK2

Figure 3

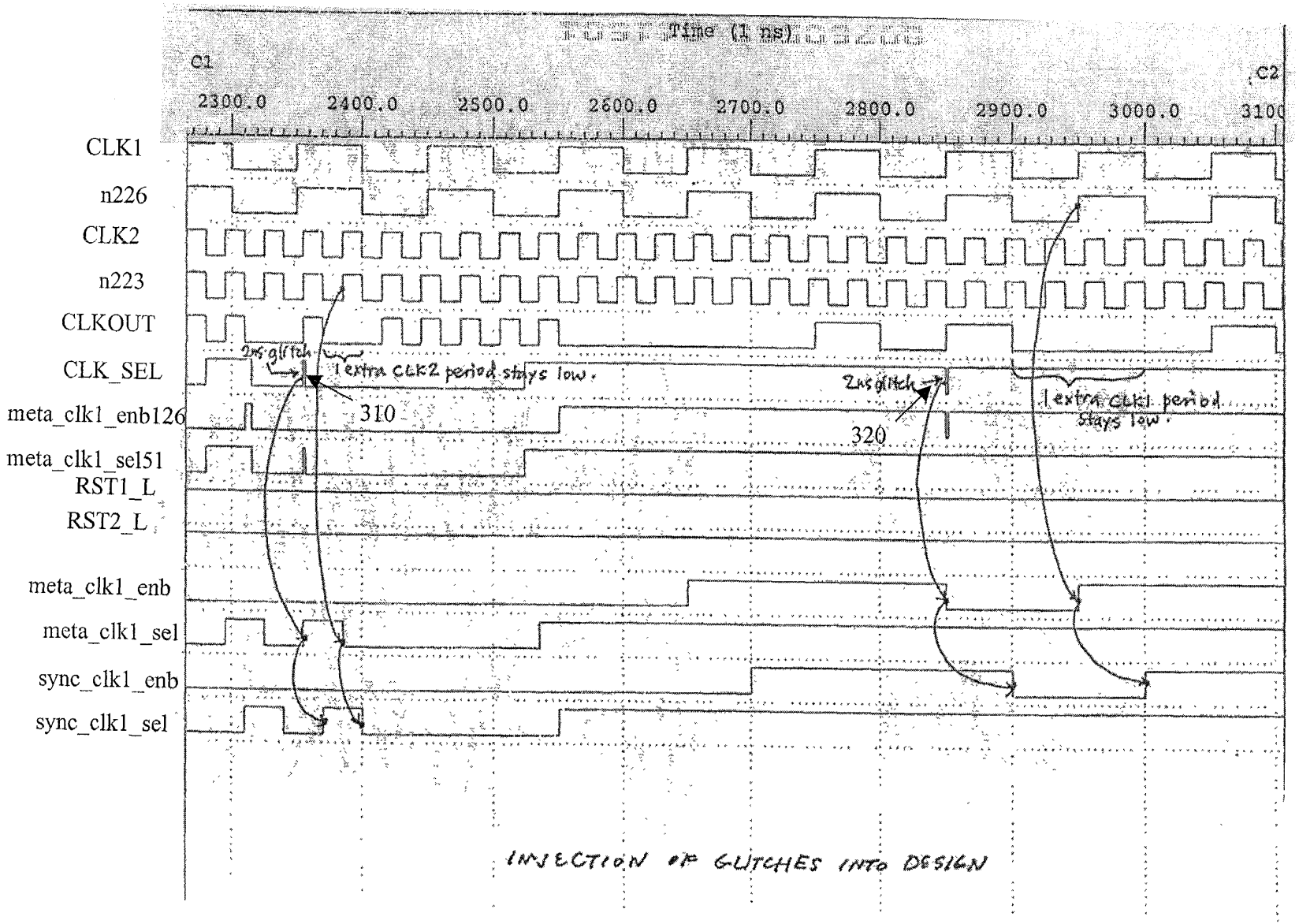

Time (1 ns)
C1
C2
2300.0
2400.0
2500.0
2600.0
2700.0
2800.0
2900.0
3000.0
CLK1
n226
CLK2
n223
CLKOUT
CLK_SEL
meta_clk1_enb126
meta_clk1_sel51
RST1_L
RST2_L
meta_clk1_enb
meta_clk1_sel
sync_clk1_enb
sync_clk1_sel
2ns glitch
1 extra CLK2 period stays low.
310
2ns glitch
320
1 extra CLK1 period stays low.
INJECTION OF GLITCHES INTO DESIGN

Figure 4

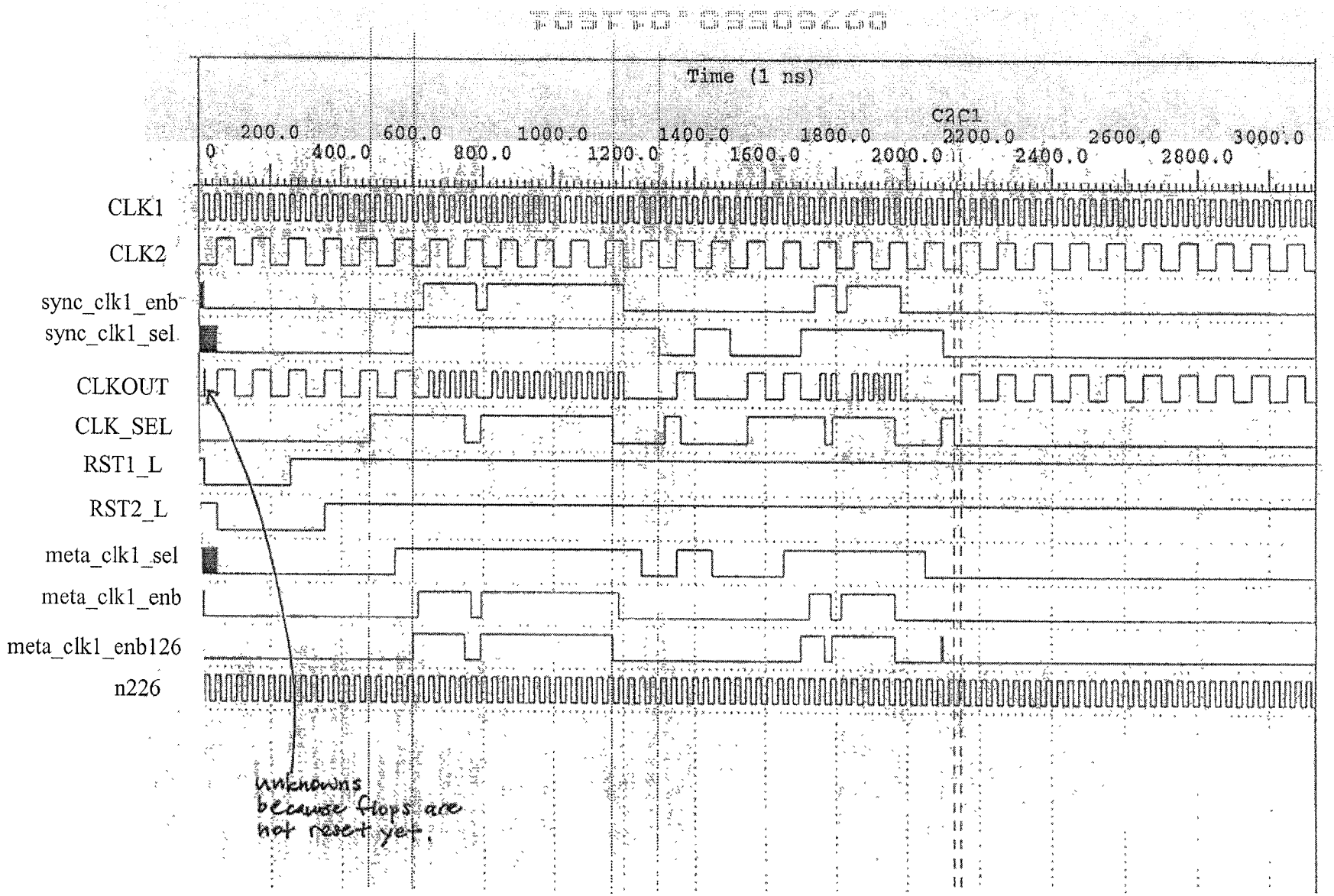


Figure 5

T1 T2 T3 T4